

Whisper Rev. BE Hardware Application Guide

KCD-0000-00

**Rev 0.3
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Kopin Corporation

125 North Drive, Westborough, MA 01581
T +1.508.870.5959, F +1.508.870.0660

PS- Rev 0.3

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1 Scope

This document details hardware interface design guideline of the Whisper SOC.

2 Power

Following table lists all the power supply requirements of the Whisper SOC.

Parameter	Min	Typ	Max	Units
VDD	1.1	1.2	1.3	Volt
VDD_IO	1.62	1.8	1.98	Volt
VDD_DSC	1.62	1.8	1.98	Volt
VDD_I2C	1.62	1.8	1.98	Volt

Following table lists power supply typical current.

Parameter		Voltage	mA
VDD		1.2	7.9
VDD_IO		1.8	0.6
VDD_DSC, Single Ended 1khz sine wav, 16Ω load	DSC_DRIVE = 1	1.8	11.4
	DSC_DRIVE = 2		21.4
	DSC_DRIVE = 3		30.1
	DSC_DRIVE = 4		37.7
	DSC_DRIVE = 5		44.4
	DSC_DRIVE = 6		50.4
	DSC_DRIVE = 7		55.5
	DSC_DRIVE = 8		60.2
VDD_DSC, Differential 1khz sine wav, 16Ω load	DSC_DRIVE = 1	1.8	10.5
	DSC_DRIVE = 2		19.8
	DSC_DRIVE = 3		27.9
	DSC_DRIVE = 4		35.2
	DSC_DRIVE = 5		41.9
	DSC_DRIVE = 6		47.9
	DSC_DRIVE = 7		53.3
	DSC_DRIVE = 8		58.4
VDD_I2C (with 2.2K pullup on I2C clock and data)		1.8	0.1

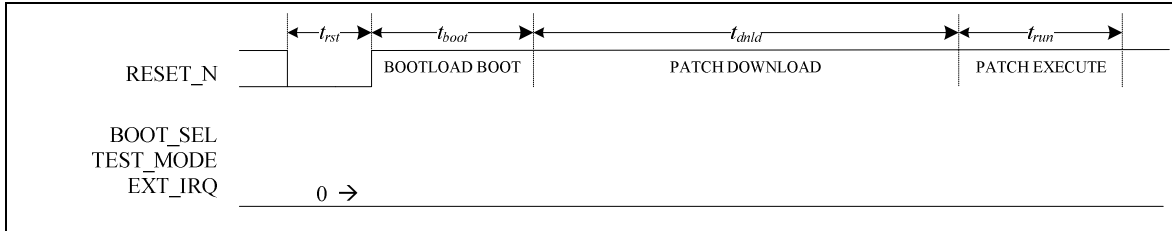
3 Clock Input

The CLK_IN requirement is listed in following table:

Parameter	Min	Typ	Max	Units
CLK_IN Frequency		24.576		MHz
CLK_IN Duty Cycle	40		60	%
CLK_IN Precision	50			ppm

4 Reset Timing

Following shows reset timing requirement. Timing is not to scale.



Parameter	I2C Clock 100Khz		I2C Clock 400Khz	
	20bytes at a time	Continuous	20bytes at a time	Continuous
t_{rst}	>= 1 μ s			
t_{boot}	1ms			
$t_{dnl'd}$	265ms	239ms	84ms	76ms
t_{run}	2ms			

5 Interfaces

5.1 I2C

The Whisper SOC supports the following I2C operation.

I2C Frequency	Device Slave Address
100Khz	0x24
400Khz	0x24

5.2 I2S

The Whisper SOC supports following configuration modes. Each I2S requires independent configuration.

I2S Mode	I2S_SCK	I2S_WS	Bit Resolution
Slave	512KHz	16KHz	16bit x 2
Slave	256KHz	8KHz	16bit x 2
Master	512KHz	16KHz	16bit x 2
Master	256KHz	8KHz	16bit x 2

5.3 SPI

The SOC incorporates both master and slave operation of SPI running up to 1MHz. It supports SPI FLASH device (Whisper is Master) and SPI Slave (External Master) bootloading.

5.4 UART1

The SOC boot status printout via UART1 via USB serial port. Port and the terminal software need to be configured for the following:

Baud Rate	Data Bits	Parity	Stop Bits	Flow Control
57600	8	N	1	None

5.5 Miscellaneous Input Pins

Following pins need to be asserted before RESET_N is released.

PIN	Board Setup
BOOT_SEL	“0”
PO_4	“0”: I2S0 is selected to output VEF audio “1”: I2S1 is selected to output VEF audio
PO_5,PO_6	“0”
EXT_IRQ	“0”

5.6 PDM

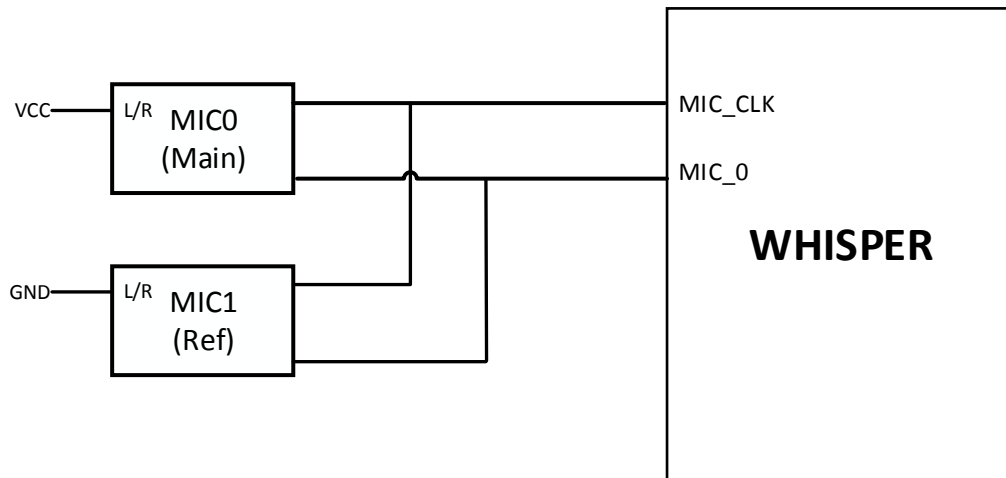
5.6.1 Recommended PDM Microphones

Following are the list of PDM microphones that are recommended.

- Knowles: SPK0415HM4H-B
- ST-Micro: MP34DT01-M
- AAC Tech: SDM0401-D263-G04

5.6.2 Recommended PDM Microphone Circuitry

Following shows how to connect PDM microphones to the Whisper. The microphones that are used in this evaluation board is from Knowles, part number SPK0415HM4H-B.

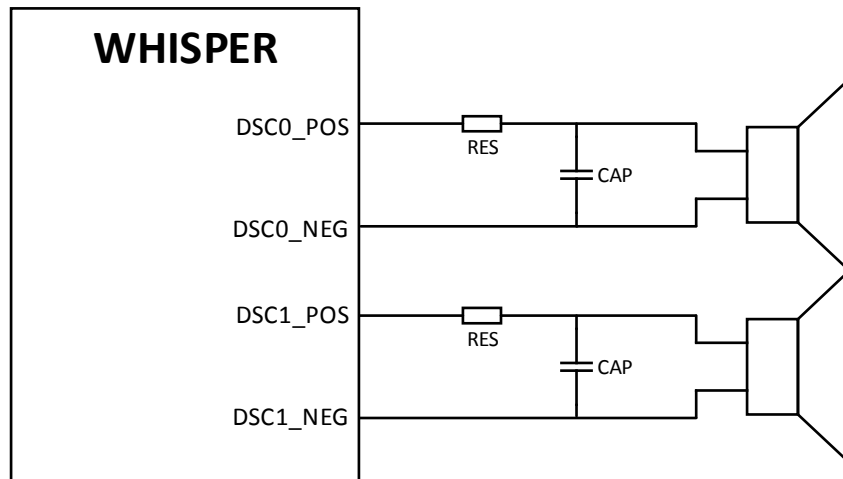


5.7 DSC™ (Digital Sound Converter)

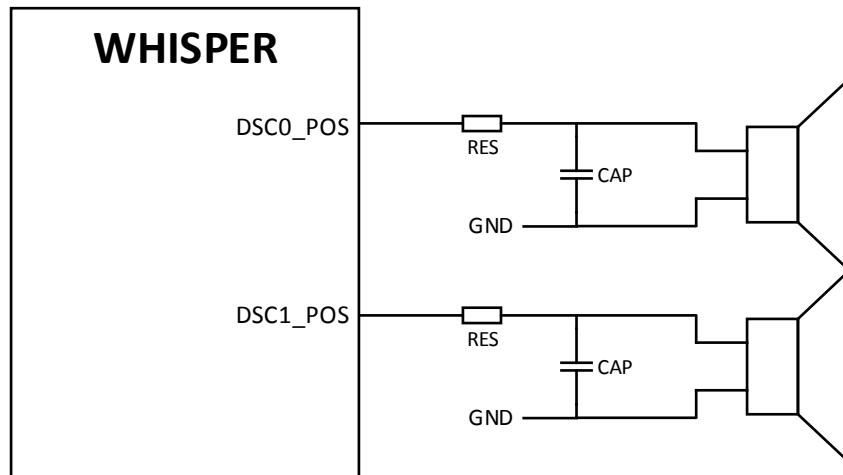
5.7.1 Recommended DSC™ Circuitry

Separate isolated ground is needed for the DSC_VSS.

Following figure shows recommended DSC™ circuitry for differential mode.



Following figure shows recommended DSC™ circuitry for single ended mode.



RC Low Pass filtering is needed for the DSC™ to operate correctly. The resistor is set to 0.1 Ohm. The value of the capacitor is chosen to have cut off frequency above 24Khz.

The resistor value is output impedance + 0.1Ohm \approx 3ohms.

$$F_C = 1/(2*\pi*R*C)$$

$$C = 1/ (2*\pi*R*F_C)$$

$$C \approx 2.2 \text{ uF}$$

Therefore, capacitor standard value of 2 uF should be sufficient. There is not much variance due to temperature or voltage across operating range.

6 Pinouts and Pin Description

Pin Name	Ball Number	Direction	Description
RESET_N	B3	IN	Global SOC Reset when "0"
CLK_IN	A5	IN	Oscillator clock in, 24.576MHz
CLK_OUT	C5	OUT	System clock out when enabled
BOOT_SEL	C4	IN	Boot select pin "1": ROM boot "0": Boot from I2C or SPI
TEST_MODE	A2	IN	"1" puts the SOC in test mode
EXT_IRQ	A3	IN	External IRQ
TRST_N	A8	IN	JTAG Reset
TMS	B8	IN	JTAG Select
TCK	C8	IN	JTAG Clock
TDI	D8	IN	JTAG Data in
TDO	C7	OUT	JTAG Data out
VAD	A4	OUT	VAD output
PO_4	E6	I/O	GPIO pin 4
PO_5	E5	I/O	GPIO pin 5
PO_6	D6	I/O	GPIO pin 6
UART0_RXD	A1	IN	UART0 RX Data
UART0_TXD	B1	OUT	UART0 TX Data
UART1_RXD	C3	IN	UART1 RX Data
UART1_TXD	C2	OUT	UART1 TX Data
I2C_SCL	G2	I/O	I2C Clock
I2C_SDA	H1	I/O	I2C Data
I2S0_SCK	H5	I/O	I2S0 Clock
I2S0_WS	E4	I/O	I2S0 Word Select
I2S0_SDI	F5	IN	I2S0 Serial Data in
I2S0_SDO	G5	OUT	I2S0 Serial Data out
I2S1_SCK	H7	I/O	I2S1 Clock
I2S1_WS	G8	I/O	I2S1 Word Select
I2S1_SDI	G7	IN	I2S1 Serial Data in
I2S1_SDO	H8	OUT	I2S1 Serial Data out
MIC_CLK_OUT	E8	OUT	2.048MHZ PDM Mic clock out
MIC_0	F6	IN	PDM0 & 1 Mic data
MIC_1	F7	IN	PDM2 & 3 Mic data
DSC0_OUT_P	H2	OUT	DSC0 Positive
DSC0_OUT_N	H3	OUT	DSC0 Negative, only valid when differential
DSC1_OUT_P	H4	OUT	DSC1 Positive
DSC1_OUT_N	G4	OUT	DSC1 Negative, only valid when differential
SPI_CLKIN	E1	IN	SPI Clock in from external Master
SPI_CLKOUT	F1	OUT	SPI Clock out from ARM Cortex M0
SPI_DIN	E3	IN	SPI data in to ARM Cortex M0
SPI_DOUT	D1	OUT	SPI data out from ARM Cortex M0
SPI_SEL_IN	D4	IN	SPI select from external master
SPI_SEL_OUT0	D2	OUT	SPI select 0 from ARM Cortex M0
SPI_SEL_OUT1	D3	OUT	SPI select 1 from ARM Cortex M0
NC	A6,A7,B6,B7,C6		No Connects

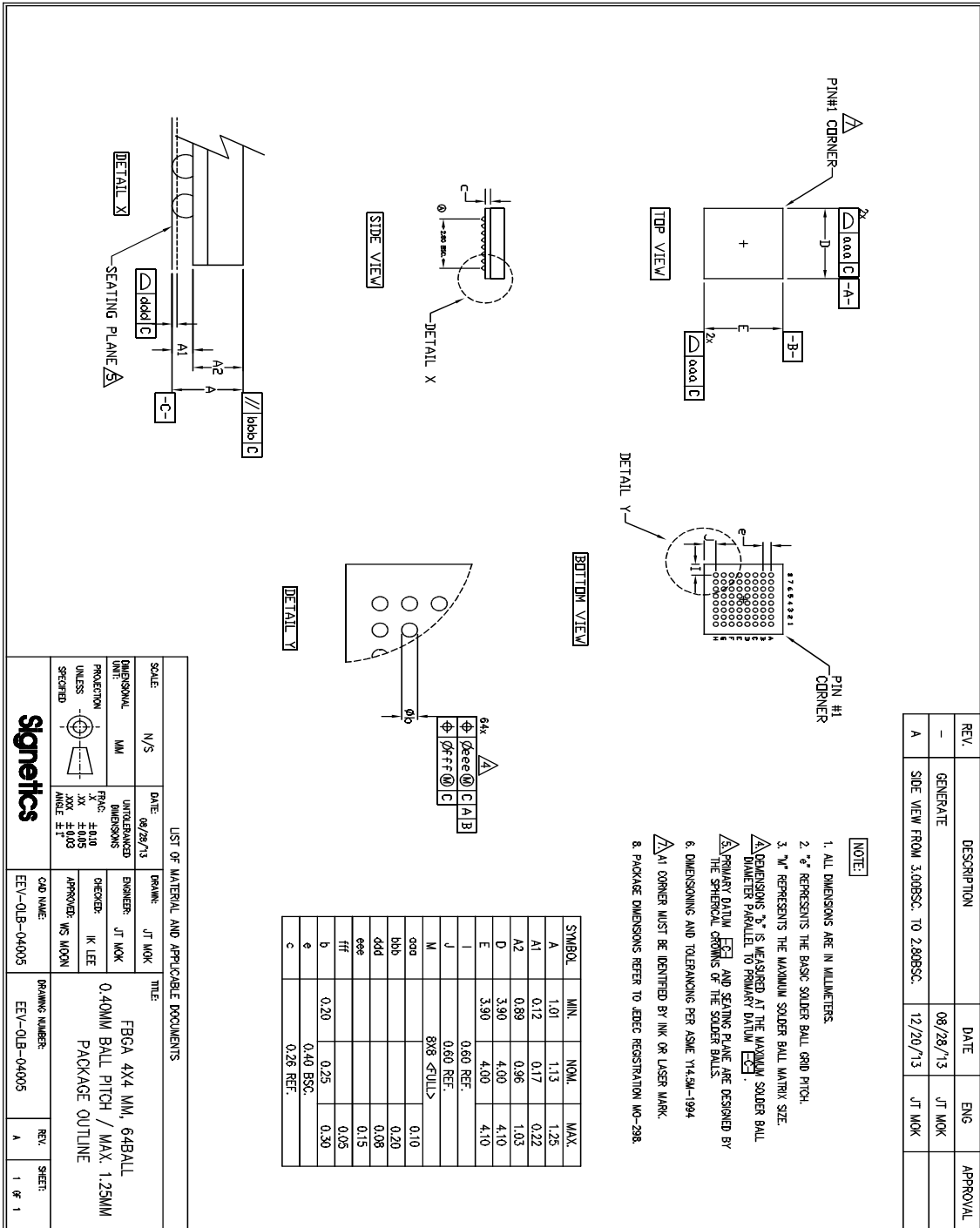
Pin Name	Ball Number	Type	Description
VDD	D5,E7,F2,H6	PWR	Core VDD, 1.2V
VSS	B2,B5,D7,G6	PWR	Core VSS
VDD_IO	C1,F4	PWR	I/O VDD, 1.8V
VSS_IO	B4,E2,F8	PWR	I/O VSS
VDD_DSC	F3	PWR	VDD for DSC Driver, 1.8V
VSS_DSC	G3	PWR	VSS for DSC Driver
VDD_I2C	G1	PWR	I2C power, 1.8V

7 Package Characteristics

7.1 Package Mechanical Data

Signetics 64 pin FPBA is used for this SOC. Following figure shows mechanical data.

Figure 1 Package Mechanical Data



8 Revision History

Revision	Date	Description
0.1	2016-07-06	Initial draft
0.2	2016-08-10	Corrections
0.3	2016-09-20	Corrections and updates